CLAIMS

We claim:

1. A method comprising:
determining a target of a branch instruction;
storing the target of the branch instruction before the branch instruction is fully executed; and
re-encountering the branch instruction and predicting a target for the branch instruction by accessing the stored target for the branch instruction.

2. The method of Claim 1, wherein the branch instruction is a direct branch.

3. The method of Claim 1, wherein the branch instruction is a backward branch.

4. The method of Claim 1, wherein storing the target comprises saving the target to a cache.

5. The method of Claim 4, wherein the target of the branch instruction is also stored in a branch prediction unit after the branch instruction has been fully executed.

6. The method of Claim 5, wherein the target is predicted for the branch instruction before the target of the branch instruction is stored in the branch prediction unit.

7. The method of Claim 6, wherein predicting a target for the branch instruction comprises:
accessing at least one target stored in at least one of the cache and the branch prediction unit;
prioritizing the accessed targets; and
generating a branch prediction based on the prioritized targets.

8. An apparatus comprising:
a decoder to determine a target of a branch instruction;
a cache to store the target of the branch instruction before the branch instruction is fully executed; and
a branch prediction unit to, upon re-encountering the branch instruction, predict the target of the branch instruction by accessing the target of the branch instruction stored in the cache.

9. The apparatus of Claim 8, wherein the decoder determines a target of a direct branch instruction.

10. The apparatus of Claim 8, wherein the decoder determines a target of a backward branch instruction.

11. The apparatus of Claim 8, wherein the branch prediction unit also stores the target of the branch instruction after the branch instruction has been fully executed.

12. The apparatus of Claim 11, wherein the branch prediction unit predicts the target for the branch instruction before the target of the branch instruction is stored in the branch prediction unit.

13. The apparatus of Claim 12, wherein the branch prediction unit predicts the target for the branch instruction by:

accessing at least one target stored in at least one of the cache and the branch prediction unit;

prioritizing the accessed targets; and

generating a branch prediction based on the prioritized targets.

14. A system comprising:

a processor capable of pipelining instructions;

a decoder to determine a target of a branch instruction to be executed by the processor;

a cache to store the target of the branch instruction before the branch instruction is fully executed by the processor; and

a branch prediction unit to, upon re-encountering the branch instruction, predict the target of the branch instruction by accessing the target of the branch instruction stored in the cache.

15. The system of Claim 14, wherein the decoder determines a target of a direct branch instruction.

16. The system of Claim 14, wherein the decoder determines a target of a backward branch instruction.

17. The system of Claim 14, wherein the branch prediction unit also stores the target of the branch instruction after the branch instruction has been fully executed.

18. The system of Claim 17, wherein the branch prediction unit predicts the target for the branch instruction before the target of the branch instruction is stored in the branch prediction unit.

19. The system of Claim 18, wherein the branch prediction unit predicts the target for the branch instruction by:

accessing at least one target stored in at least one of the cache and the branch prediction unit;

prioritizing the accessed targets; and

generating a branch prediction based on the prioritized targets.